## REMARKS

The following is responsive to the Official Action mailed on April 17, 2006, and for which a three-month extension is hereby requested. The Office Action allowed claim 33 and rejected the other pending claims. Claims 19, 20, 22, and 28-31 have been amended to have their dependence changed so that they now all have claim 33 as their base claim and, consequently, should also now be allowable. The other previously pending claims have been cancelled. New claims 42-52 have been added.

New claims 42-47

Claims 42-47 are primarily drawn to the write protection aspects of the present invention described principally in section V of the application that begins on page 52 at line 15. Independent claim 42 presents a memory system that can be connected to any of a plurality of hosts and which includes an interface, a memory having memory cells and write circuitry for storing data in the cells, a controller, and a set of registers connected to the controller.

Claim 42 includes several features that are not believed to be found in the prior art. A first of these is that amongst the information for the management of the memory stored of in registers is a parameter indicating the size of the memory groups, a limitation not found in the previously claims.

Other features of claim 42 include the memory having

> a plurality of group tags, each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells of the corresponding memory group are write protected ..., wherein any combination of the memory groups can be write protected

and that

> said group tags are settable in response to a command from the host to which the memory system is connected.

These features are also not believed to be found in the prior art. These limitations are similar to those found in previously pending claim 37, which the Office Action rejected; however, as discussed in the previous response, this rejection is believed to be incorrect.

More specifically, the Office Action cited the "Flash Memory Products, 1992/1993 Data Book/Handbook, Advanced Micro Devices, Am29F010 ("AMD"). The AMD reference does have some discussion of write protection on page 1-10. However, as is clear from the "Sector Protection" section on that page, the ability to disable the program operation in sectors of the AMD

device is *hardware* sector protection. It does not employ tags, but relies entirely on the hardware structure described in this section of AMD. Further, in AMD the ability to write protect is *not* "in response to a command from a host to which the memory system is connected"; rather, as is again clear for AMD's "Sector Protection", to write protect a sector must either be done as the manufacture or by using special programming equipment. This is no disclosure of a host to which the memory system is connected to receive date being able to perform such a process.

New dependent claim 43 adds the limitation of "wherein the value of the parameter indicating the size of the memory groups is configurable by the host to which the card is connected" and is believed to be further allowable on this basis. This limitation is similar to those found in previously pending 24, for which the Office Action cited Hazen et al. (U.S. patent number 5,280,447) or Lee et al. (U.S. patent number 5,796,657); however, as discussed in the previous response, this rejection is believed to be incorrect. First, it should be noted that AMD teaches away from any such configurability and the unit that can be write protected is the sector, a unit fixed in the hardware design of the device. For the Hazan reference, the Office Action cites column 4, lines 39-42; but the cited portions of Hazan are again all concerned with *erase* structures, not *write* protection. Similarly, for the Lee reference, the Office Action cites column 3, lines 30-40, and column 5, lines 13-16; but the cited portions of Lee are again all concerned with *erase* structures, not *write* protection. Neither Hazan nor Lee disclose "the number of memory cells in each memory group is configurable" for write protection groups.

New dependent claim 44 adds the limitation of "wherein said group tags are deselected in response to command from said host", and is believed to be further allowable on this basis. This limitation is similar to those found in previously pending 38, for which the Office Action cites AMD page 1-10, which does refer to write protection; however, it has no disclosure of deselecting protected areas. In particular, it has no disclosure of deselecting "in response to command from said host." This section of AMD only a *hardware* protection and only to set the protection, a process not done by a host but which needs to done at the factory or with special equipment.

Similarly, dependent claims 45-47 are also all believed further allowable for the additional limitations they recite.

New claims 48-52

Claims 48-52 are primarily draw to the erase aspects of the present invention described principally in section IV of the application that begins on page 48 at line 12. Independent claim 48 presents a memory system that can be connected to any of a plurality of hosts and which includes an interface, a memory having memory cells and erase circuitry, a controller, and a set of registers connected to the controller.

Claim 48 includes several features that are not believed to be found in the prior art. The structure found in these claims describes a memory that has a plurality of groups; each group has a plurality of sectors/units of erase; and each sector/unit of erase is composed of multiple cells. Thus, there are *two* levels of structure between the cell and the memory, the group and the sector/unit of erase, with a tag for each of the elements at *both* of these levels. Any combination of groups, and any combination of sectors/units of erase in any group, can have their erase tag set in response to host commands and then all erased simultaneously. Further, another feature not believed to be found in the prior art is that amongst the information for the management of the memory stored of in registers is a parameter indicating number of memory sectors in each of the memory groups, a limitation not found in the previously claims.

These limitations are similar to those found in previously in the combination of claims 18, 28, and 29, which the Office Action rejected; however, as discussed in the previous response, these rejections are believed to be incorrect.

More specifically, the Office Action cited AMD in view of Kaki et al (U.S. patent 5,809,515). Concerning the AMD reference, beginning on page 1-3, this describes a first device (Am29F010) that is composed on multiple sectors. As described on page 1-3 and, in more detail, on pages 1-11 and 1-12, this device can be erased at the chip level and at the sector level for multiple sectors. However, it only has this single intermediate level of the sector between the cell level and the entire chip. There is neither disclosure nor suggestion of another intermediate layer corresponding to the "group" of the claims. Beginning on page 3-38, AMD presents a *different* device (AmC002FLKA). As described on page 3-48, this device only erases at the level of the entire array and on 256K byte segments. There is also neither disclosure nor suggestion of another intermediate layer corresponding to the "group" of the claims for this device. In its comments, the Office Action refers to the "memory groups" of the claims

corresponding to S0-S7 on page 3-39, further stating that each of these S0-S7 have a plurality of sectors as disclosed on page 1-4. It is again noted that the device on page 3-39 *is a different device* from that found on page 1-4. Further, there is no disclosure in AMD the S0-S7 have any sort of association with what is defined by the claims as a "group".

As for the Kaki reference, this also only describes the structure of a chip having multiple sectors (the unit of erase), where each sector has multiple cells. Kaki neither discloses nor suggests the introduction of another intermediate layer corresponding to the "group" of the claims. Beginning at line 64 of column 7, Kaki considers where there unit of erase may be a different size than a sector (this is done for consideration of how it affects the "write management table"), but still only considers a single intermediate level (the erase unit) between the entire array and the cell. There is again no discussion of the concurrent use of a second, distinct intermediate level corresponding to the "group" of the claims.

Further, as for "any combination of the memory groups can be simultaneously erased", this is not only *not* taught by Kaki, but is *directly contrary* to what Kaki teaches. In its comments, the Office Action refers column 7, lines 28-30, which state "the plurality of flash memories 4 are erased in parallel"; however, these are different memory arrays that are erased in parallel. As described with respect to Figure 4 beginning at line 32 of column 7, for each of these parallel erase operations only a single sector/unit of erase is being erased at a time; that is, within a given flash memory 4, the sectors are erased *sequentially* and only one sector at time can be erased. In Figure 4 of Kaki, this is function of the loop from diamond 45 back up to above boxes 43 and 44. In Kaki, the in "parallel" is for different arrays, but in each array the units of erase are only done sequentially as is clear from text.

Further, another feature of claim 48 not believed to be found in the prior art is that amongst the information for the management of the memory stored of in registers is a parameter indicating number of memory sectors in each of the memory groups, a limitation not found in the previously claims.

New dependent claim 49 adds the limitation of "wherein the corresponding sectors in each memory group is calculated in real time", and is believed to be further allowable on this basis. This limitation is similar to those found in previously pending 19, for which the Office Action cites AMD at 1-25. However, this section of AMD is about *protection* of sectors from erase, not arranging of sectors in "group" structure so that they *can* be erased. Also, this is a

*hardware* arrangement that either must be done at the factor or using special equipment (see AMD page 1-10); consequently, it is not something that can be performed "in real time". Further, as already discussed, AMD lacks any corresponding "group" structure and all arrangements of erase structures are fixed in hardware according to the design, so that there is no such corresponding concept to even be computed, whether in real time or otherwise.

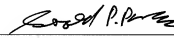
New dependent claim 51 adds the limitation of "wherein said ones of said sector tags and said group tags are deselectable in response to a command from the host to which the memory system is connected", and is believed to be further allowable on this basis. This limitation is similar to those found in previously pending 30, for which the Office Action cites AMD at 1-25. However, this section of AMD is about *protection* of sectors from erase, *not* the selecting and deselecting of sectors or "groups" so that they *can* be erased. Also, this is a *hardware* arrangement that either must be done at the factor or using special equipment (see AMD page 1-10); consequently, it is not something done "in response to a host command".

New dependent claim 52 adds the limitation of "wherein the number of memory sectors in each memory group is configurable by a host to which the memory system is connected", and is believed to be further allowable on this basis. This limitation is similar to those found in previously pending 31, for which the Office Action cites AMD at 1-25. However, this section of AMD is about *protection* of sectors from erase, not arranging of sectors into a "group" structure so that they *can* be erased. Also, this is a *hardware* arrangement that either must be done at the factor or using special equipment (see AMD page 1-10); consequently, it is not something that can be performed by a host. Further, as already discussed, AMD lacks any corresponding "group" structure and all arrangements of erase structures are fixed in hardware according to the design, so that they cannot be configured as described in the claim.

Conclusion

Therefore, for any of the above reasons, it is respectfully submitted that claims 19, 22, 28-31, 33, and 42-52 are allowable over the prior art. Consideration of claims 42-52 and an early indication of their allowance are respectfully requested.

Respectfully submitted,



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